CLAIMS

1. A method of filling an isolation trench formed in a semiconductor substrate; said method comprising:

depositing an insulating liner layer at least along sidewalls and a bottom of said isolation trench;

forming a silicon liner layer atop said insulating liner layer that lines said sidewalls and bottom of said isolation trench;

removing an upper portion of said insulating liner layer;

removing said silicon liner layer; and

filling at least an upper portion of said trench with another insulating layer.

2. The method of claim 1 wherein a thickness of said insulating liner layer and a thickness of said silicon liner layer are selected such that said another insulating layer fills said upper portion of said trench without voids.

3. The method of claim 1 wherein said insulating liner layer is an oxide.

4. The method of claim 1 wherein said step of depositing an insulating liner layer includes a low pressure chemical vapor deposition (LPCVD) of said insulating liner layer.

5. The method of claim 1 further comprising forming an oxide layer along sidewalls and a bottom region of said isolation trench and depositing a nitride layer atop said first insulating liner layer prior to depositing said insulating liner layer.

6. The method of claim 5 wherein said oxide liner layer has a thickness of 10 to 300 Å, and said nitride layer has a thickness of 20 to 300 Å.

7. The method of claim 1 wherein said step of depositing an insulating liner layer includes depositing a portion of said insulating liner layer at least above a top of said trench; and said step forming a silicon liner layer includes depositing said silicon liner layer at least above

said portion of said insulating liner layer that extends above said top of said trench, and planarizing said silicon liner layer to said top of said insulating liner layer.

8. The method of claim 1 wherein said step of depositing a silicon liner layer includes a low pressure chemical vapor deposition (LPCVD) of said silicon liner layer.

9. The method of claim 1 wherein said silicon liner layer is selected from the group consisting of polysilicon and amorphous silicon.

10. The method of claim 1 wherein said step of removing an upper portion of said insulating liner layer comprises removing at least an upper 100 to 2000 Å of said insulating liner layer.

11. The method of claim 1 wherein said step of removing an upper portion of said insulating liner layer includes at least one of a wet etch and a plasma etch of said insulating liner layer.

12. The method of claim 1 wherein said step of removing at least an upper portion of said silicon liner layer includes at least one of a wet etch and a plasma etch of said silicon liner layer.

13. The method of claim 1 wherein said another insulating layer comprises a high density plasma (HDP) deposited oxide.

14. A method of filling an isolation trench formed in a semiconductor substrate; said method comprising:

forming a first oxide liner layer having a thickness of 10 to 300 Å along sidewalls and a bottom region of said isolation trench;

depositing a nitride liner layer having a thickness of 20 to 300 Å atop said first oxide liner layer; and

depositing a further oxide liner layer atop said nitride liner layer;

depositing a silicon liner layer atop said further oxide liner layer, said silicon liner layer being selected

from the group consisting of polysilicon and amorphous silicon;

planarizing said silicon liner layer to said top of said further oxide liner layer;

removing at least an upper 100 to 2000 Å portion of said further oxide liner layer;

removing said silicon liner layer; and

filling at least an upper portion of said trench with another oxide layer;

a thickness of said further oxide liner layer and a thickness of said silicon liner layer being selected such that said another oxide layer fills an upper portion of said trench without voids.

15. A method of filling an isolation trench formed in a semiconductor substrate; said method comprising:

(a) depositing an insulating liner layer at least along sidewalls and a bottom of said isolation trench;

(b) forming a silicon liner layer atop said insulating liner layer that lines said sidewalls and said bottom of isolation trench;

(c) repeating steps (a) and (b) until said trench is filled;

(d) removing an upper portion of said insulating liner layer;

(e) removing an upper portion of said silicon liner layer; and

(f) filling at least an upper portion of said trench with another insulating layer.

16. The method of claim 15 wherein a thickness of said insulating liner layer and a thickness of said silicon liner layer are selected such that said another insulating layer fills said upper portion of said trench without voids.

17. The method of claim 15 wherein said insulating liner layer is an oxide.

18. The method of claim 15 wherein said step of depositing an insulating liner layer includes a low pressure

chemical vapor deposition (LPCVD) of said insulating liner layer.

19. The method of claim 15 further comprising forming an oxide layer along sidewalls and a bottom region of said isolation trench and depositing a nitride layer atop said first insulating liner layer prior to depositing said insulating liner layer.

20. The method of claim 19 wherein said oxide layer has a thickness of 10 to 300 Å, and said nitride layer has a thickness of 20 to 300 Å.

21. The method of claim 15 wherein said step of depositing an insulating liner layer includes depositing a portion of said insulating liner layer at least above a top of said trench; said step forming a silicon liner layer includes depositing said silicon liner layer at least above said portion of said insulating liner layer that extends above said top of said trench and planarizing said silicon liner layer to said top of said insulating liner layer.

22. The method of claim 15 wherein said step of depositing a silicon liner layer includes a low pressure chemical vapor deposition (LPCVD) of said silicon liner layer.

23. The method of claim 15 wherein said silicon liner layer is selected from the group consisting of polysilicon and amorphous silicon.

24. The method of claim 15 wherein said step of removing an upper portion of said insulating liner layer comprises removing at least an upper 100 to 2000 Å of said insulating liner layer.

25. The method of claim 15 wherein said step of removing an upper portion of said insulating liner layer includes at least one of a wet etch and a plasma etch of said insulating liner layer.

26. The method of claim 15 wherein said step of removing an upper portion of said silicon liner layer includes at least one of a wet etch and a plasma etch of said silicon liner layer.

27. The method of claim 15 wherein said another insulating layer comprises a high density plasma (HDP) deposited oxide.

28. The method of claim 15 further comprising depositing at least one further insulating liner layer atop said silicon liner layer prior to removing said insulating liner layer; and depositing at least one further silicon liner layer atop said further insulating liner layer.

29. A method of filling an isolation trench formed in a semiconductor substrate; said method comprising:

(a) forming a first oxide liner layer having a thickness of 10 to 300 Å along sidewalls and a bottom region of said isolation trench;

(b) depositing a nitride liner layer having a thickness of 20 to 300 Å atop said first oxide liner layer that lines the sidewalls and bottom of the isolation trench; and

(c) depositing a further oxide liner layer;

(d) depositing a silicon liner layer atop said further oxide liner layer, said silicon liner layer being selected from the group consisting of polysilicon and amorphous silicon;;

(e) planarizing said silicon liner layer to a top of said further oxide liner layer;

(f) repeating steps (c), (d) and (e) until said isolation trench is filled;

(g) removing at least an upper 100 to 2000 Å portion of said further oxide liner layers;

(h) removing upper portions of said silicon liner layers; and

(i) filling at least an upper portion of said trench with another oxide layer;

a thickness of said further oxide liner layer and a thickness of said silicon liner layer being selected such that said another oxide layer fills said upper portion of said trench without voids.

30. An isolation structure formed within an isolation trench in a semiconductor substrate, said isolation trench having sidewalls and a bottom region; said isolation structure comprising:

at least two insulating liner layers formed along a lower portion of said sidewalls and along said bottom region of said isolation trench;

at least one silicon liner layer formed between said at least two insulating liner layers at a portion that lines said bottom of said isolation trench; and

another insulating layer that fills a remaining portion of said trench.

31. The isolation structure of claim 30 wherein said at least two insulating liner layers are an oxide.

32. The isolation structure of claim 30 further comprising:

an oxide layer formed along sidewalls and a bottom region of said isolation trench; and

a nitride layer formed atop said first insulating liner layer;

a first one of said insulating liner layers being formed atop a lower portion of said nitride layer.

33. The isolation structure of claim 32 wherein said oxide layer has a thickness of 10 to 300 Å, and said nitride layer has a thickness of 20 to 300 Å.

34. The isolation structure of claim 30 wherein said silicon liner layer is selected from the group consisting of polysilicon and amorphous silicon.

35. The isolation structure of claim 30 wherein said insulating liner layers cover all of said sidewalls except for an uppermost 100 to 2000 Å.

36. An isolation structure formed within an isolation trench in a semiconductor substrate, said isolation trench having sidewalls and a bottom region; said isolation structure comprising:

an oxide layer having a thickness of 10 to 300 Å formed along said sidewalls and said bottom region of said isolation trench;

a nitride layer having a thickness of 20 to 300 Å formed atop said first oxide liner layer; and

at least two insulating liner layers formed atop a lower portion of said nitride liner layer, said insulating liner layers being an oxide, said lower portion comprising all of said sidewalls except for at least an uppermost 100 to 2000 Å;

at least one silicon liner layer formed between said at least two insulating liner layers at a portion that lines said bottom of said isolation trench, said silicon liner layer being selected from the group consisting of polysilicon and amorphous silicon; and

another oxide layer that fills a remaining portion of said trench;

a thickness of said further oxide liner layer and a thickness of said silicon liner layer being selected such that said another oxide layer fills an upper portion of said trench without voids.